FIG 1

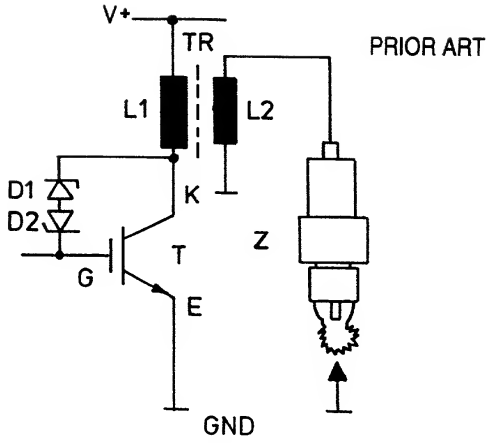
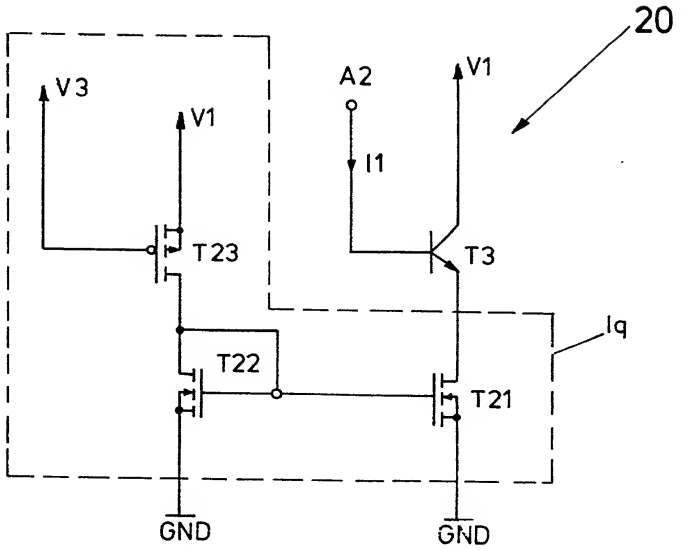

V+
TR
PRIOR ART
L1
L2
D1
D2
K
T
Z
G
E
GND

FIG 5


20
V3
V1
A2
V1
I1
T23
T3
Iq
T22
T21
GND
GND

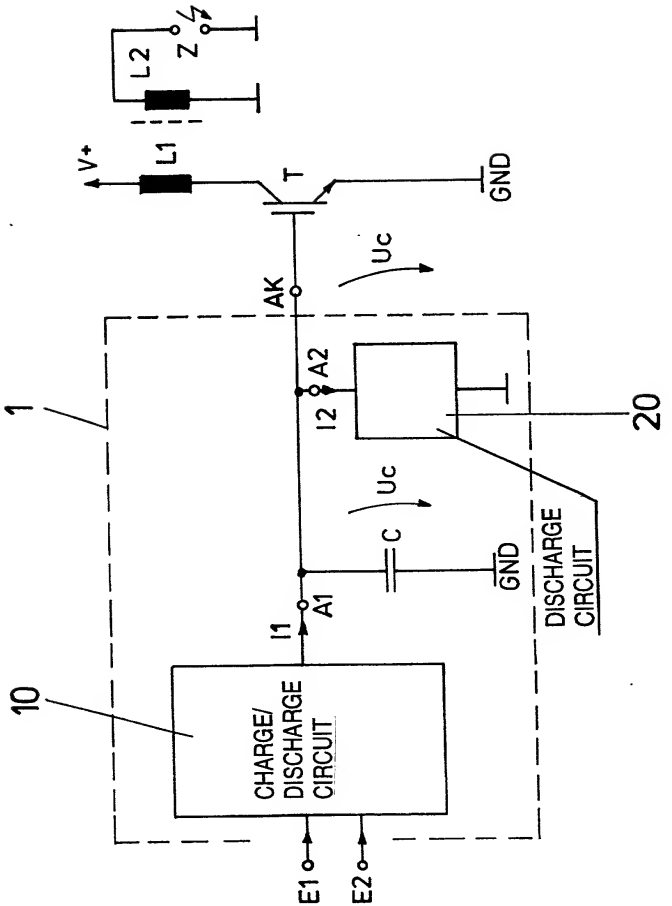

L2
Z
V+
L1
T
GND
AK
Uc
1
A2
I2
20
Uc
C
GND
DISCHARGE
CIRCUIT
I1
A1
10
CHARGE/
DISCHARGE
CIRCUIT
E1
E2

FIG 2

FIG 3

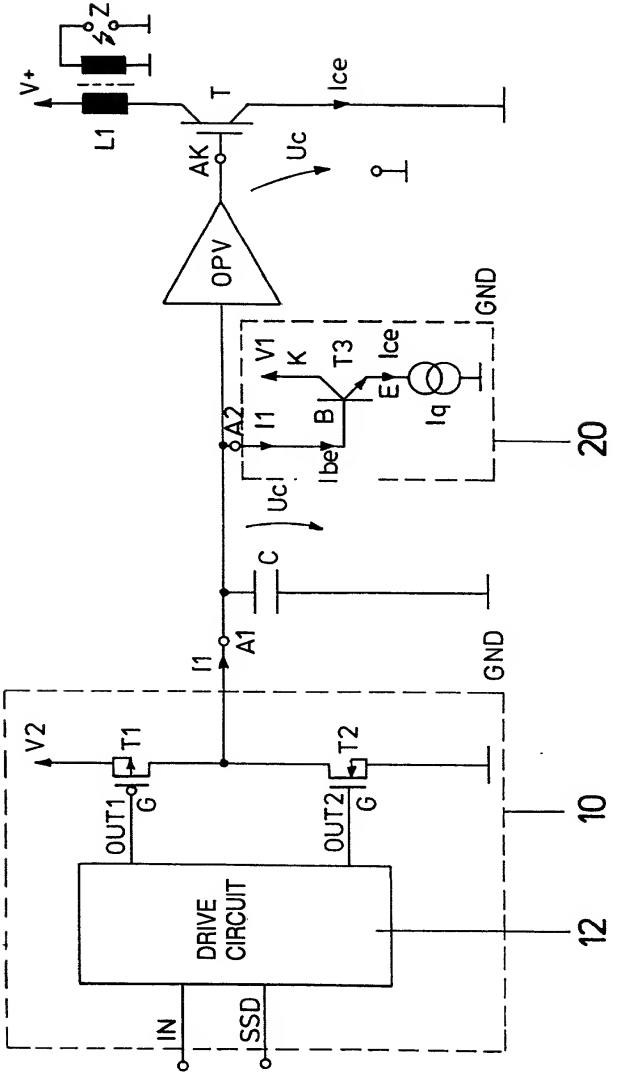

Z
V+
L1
T
Ice
AK
Uc
OPV
GND
V1
K
T3
Ice
E
Iq
A2
I1
B
Ibe
Uc
20
C
A1
I1
GND
V2
T1
T2
OUT1
G
OUT2
G
10
DRIVE CIRCUIT
12
IN
SSD

FIG. 4A

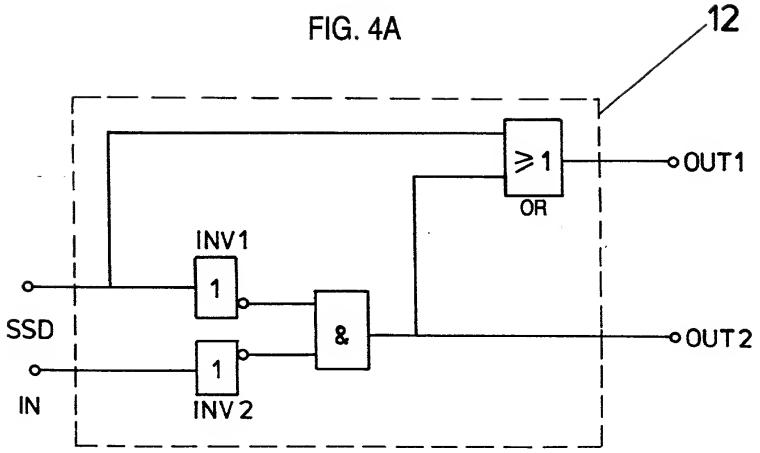


FIG. 4B

IN	SSD	OUT1	OUT2
1	1	1	0
1	0	0	0
0	1	1	0
0	0	1	1

FIG 6 A

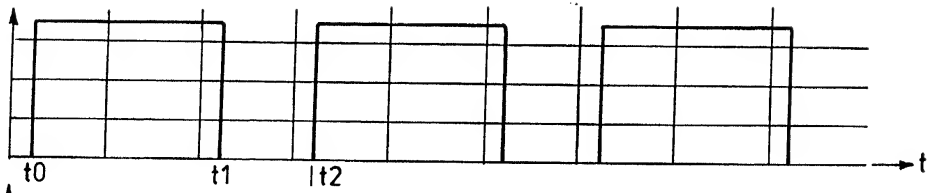


FIG 6 B

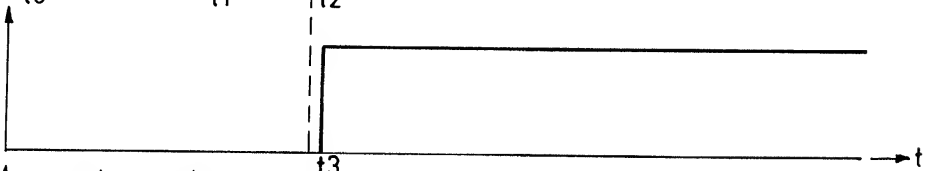


FIG 6C

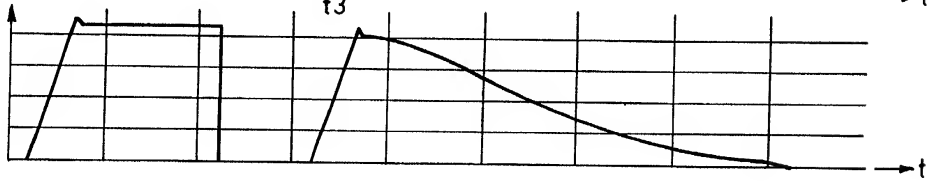
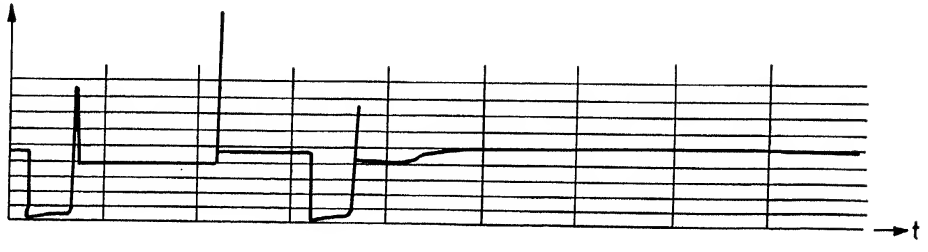



FIG 6D